In the Claims:

1. (Previously Presented) An electronic component comprising:

a wafer;

a plurality of bond pads disposed on a surface of the wafer;

a plurality of functional 3-D structures disposed on the surface of the wafer, such that each bond pad is laterally spaced from the plurality of bond pads so that each bond pad is associated with a laterally-spaced one of the 3-D structures, each functional 3-D structure including a non-conductive compliant base element and having an upper surface spaced from the surface of the wafer;

a plurality of reroute traces, each reroute trace extending over the surface of the wafer between a bond pad and its associated 3-D structure such that each reroute trace is electrically connected to one of the bond pads and extends onto the upper surface of the associated laterally-spaced one of the functional 3-D structures so that the reroute trace provides an electrical connection between the bond pad and the upper surface of the associated functional 3-D structure; and

a plurality of selected 3-D structures disposed on the surface of the wafer to provide a mechanical reinforcement, wherein at least some of the selected 3-D structures have a greater mechanical load-bearing capacity than some of the functional 3-D structures.

2. (Original) The component of claim 1 wherein each reroute trace comprises a copper/nickel layer that is covered by a gold layer.

3. (Original) The component of claim 1 wherein the selected 3-D structures have a lower degree of compressibility than the functional 3-D structures.

4. (Previously Presented) The component of claim 1 wherein the selected 3-D structures have a greater height than the functional 3-D structures.

5. (Previously Presented) The component of claim 1 wherein each of the selected 3-D structures includes a compliant base element that has a greater volume than the compliant base element of the functional 3-D structures.

6-7. (Cancelled)

8. (Original) The component of claim 1 wherein the selected 3-D structures are arranged in a regularly distributed manner in an edge region of the wafer.

9. (Original) The component of claim 1 wherein the selected 3-D structures are arranged in a regularly distributed manner over the wafer.

10. (Original) The component of claim 1 wherein the selected 3-D structures are able to be electrically bonded.

11-33. (Cancelled)

34. (Previously Presented) The electronic component of claim 1, wherein the compliant base element is formed from silicone.

35. (Previously Presented) The component of claim 1 wherein each of the selected 3-D structures is protected by a metal cap.

36. (Previously Presented) The component of claim 1 wherein each of the selected 3-D structures is surrounded by a metallic supporting ring.

37. (New) The component of claim 1 wherein each of the selected 3-D structures have a support structure formed upon a surface of the wafer.

38. (New) The component of claim 37 wherein the support structure comprises a metal ring formed along side surfaces of the selected 3-D structures.

39. (New) The component of claim 38 wherein the metal ring is not disposed on any portion of an upper surface of the selected 3-D structures.

40. (New) The component of claim 37 wherein the support structure is formed from the same material as the reroute traces.

41. (New) The component of claim 37 wherein each reroute trace comprises a copper/nickel layer that is covered by a gold layer.

42. (New) The component of claim 37 wherein the selected 3-D structures have a lower degree of compressibility than the functional 3-D structures.

43. (New) The component of claim 37 wherein the selected 3-D structures have a greater height than the functional 3-D structures.

44. (New) The component of claim 37 wherein each of the selected 3-D structures includes a compliant base element that has a greater volume than the compliant base element of the functional 3-D structures.

45. (New) The component of claim 37 wherein the selected 3-D structures are arranged in a regularly distributed manner in an edge region of the wafer.

46. (New) The component of claim 37 wherein the selected 3-D structures are arranged in a regularly distributed manner over the wafer.